

CLAIMS

What is claimed is:

- 1 1. A content addressable memory (CAM) system comprising:
2 a first CAM device having a priority number output and a first enable input;
3 a second CAM device having a priority number input and an enable output coupled to the
4 priority number output and the first enable input, respectively, of the first CAM
5 device, the second CAM device further having a priority number output and an
6 enable input; and
7 a third CAM device having a priority number input and an enable output coupled to the
8 priority number output and the enable input, respectively, of the second CAM device.
- 1 2. The system of claim 1 wherein the first CAM device additionally has a second enable input
2 coupled to the enable output of the third CAM device.
- 1 3. The system of claim 1 further comprising an output bus coupled to each of the first, second
2 and third CAM devices.
- 1 4. The system of claim 3 wherein the third CAM device comprises:
2 a CAM core to output a local match address and a local priority value in response to a
3 compare instruction; and
4 a cascade logic circuit coupled to receive the local priority value from the CAM core and a
5 remote priority value via the priority number input of the third CAM device, the
6 cascade logic circuit being configured to output an enable signal via the enable output
7 of the third CAM device if the remote priority value has a higher priority than the

8 local priority value and to enable the local match address to be output onto the output
9 bus if the local priority value has a higher priority than the remote priority value.

1 5. The system of claim 3 wherein the second CAM device comprises:

2 a CAM core to output a local match address and a local priority value in response to a
3 compare instruction; and
4 a cascade logic circuit coupled to receive the local priority value from the CAM core and a
5 remote priority value via the priority number input of the second CAM device, the
6 cascade logic circuit being configured to output an enable signal via the enable output
7 of the second CAM device if the remote priority value has a higher priority than the
8 local priority value and to enable the local match address to be output onto the output
9 bus if (1) the local priority value has a higher priority than the remote priority value
10 and (2) if an enable signal is received via the enable input of the second CAM device.

1 6. The system of claim 5 wherein the cascade logic circuit is further configured to output the
2 remote priority value via the priority number output of the second CAM device if the
3 remote priority value has a higher priority than the local priority value and to output the
4 local priority value via the priority number output of the second CAM device if the local
5 priority value has a higher priority than then remote priority value.

1 7. The system of claim 3 wherein the first device comprises:

2 a CAM core to output a local match address and a local priority value in response to a
3 compare instruction; and
4 a cascade logic circuit to receive the local priority value from the CAM core and
5 configured to output the local priority value via the priority number output of the first

6 CAM device, the cascade logic being further configured to enable the local match
7 address to be output onto the output bus if an enable signal is received via the first
8 enable input of the first CAM device.

1 8. The system of claim 1 further comprising an output bus coupled to each of the first, second
2 and third CAM devices and wherein the first CAM device additionally has:
3 a second enable input coupled to the enable output of the third CAM device;
4 a CAM core to output a local match address in response to a compare instruction; and
5 a cascade logic circuit to enable the local match address to be output onto the output bus if
6 (1) a first enable signal is received via the first enable input of the first CAM device
7 and (2) a second enable signal is received via the second enable input of the first
8 CAM device.

1 9. A content addressable memory (CAM) system comprising:
2 a first CAM device to output a first priority value;
3 a second CAM device coupled to receive the first priority value from the first CAM device
4 and configured to output, as a winning priority value, a highest priority one of the
5 first priority value and a second priority value; and
6 a third CAM device coupled to receive the winning priority value from the second CAM
7 device and configured to output a first enable signal to the second CAM device if the
8 winning priority value has a higher priority than a third priority value.

1 10. The system of claim 9 further comprising an enable line coupled between the second and
2 third CAM devices to conduct the first enable signal from the third CAM device to the
3 second CAM device, and wherein the enable line is additionally coupled to the first CAM

4 device to conduct the first enable signal thereto.

1 11. The system of claim 10 wherein the second CAM device is further configured to output a
2 second enable signal to the first CAM device if the first priority value is the winning
3 priority value.

1 12. The system of claim 9 wherein the second CAM device is further configured to output a
2 second enable signal to the first CAM device if (1) the first priority value is the winning
3 priority value and (2) the first enable signal is output by the third CAM device.

1 13. The system of claim 9 wherein the first CAM device includes a first CAM core to generate
2 a first match address that corresponds to the first priority value, the second CAM device
3 includes a second CAM core to generate a second match address that corresponds to the
4 second priority value, and the third CAM device includes a third CAM core to generate a
5 third match address that corresponds to the third priority value.

1 14. The system of claim 13 wherein the third CAM device is further configured to output the
2 third match address onto an output bus if the third priority value has a higher priority than
3 the winning priority value.

1 15. The system of claim 14 wherein the second CAM device is further configured to output the
2 second match address onto the output bus if the third CAM device outputs the first enable
3 signal and the second priority value is the winning priority value.

1 16. The system of claim 15 wherein the first CAM device is coupled to receive the first enable
2 signal from the third CAM device, and wherein the second CAM device is further

3 configured to output a second enable signal to the first CAM device if the first priority
4 value is the winning priority value, and wherein the first CAM device is further configured
5 to output the third match address onto the output bus if (1) the first CAM device outputs
6 the first enable signal and (2) the second CAM device outputs the second enable signal.

1 17. The system of claim 14 wherein the second CAM device is further configured to output a
2 second enable signal to the first CAM device if the third CAM device outputs the first
3 enable signal and the first priority value is the winning priority value, and wherein the first
4 CAM device is further configured to output the third match address onto the output bus in
5 response to the second enable signal.

1 18. The system of claim 13 wherein each of the first, second and third CAM cores comprises a
2 respective CAM array and a respective priority storage array and is configured to:
3 compare a first comparand value with contents of the CAM array to identify one or more
4 local priority values within the priority storage array;
5 output a highest priority one of the one or more local priority values from the priority
6 storage array; and
7 generate a match address that identifies a storage location within the CAM array that
8 corresponds to the highest priority one of the one or more local priority values.

1 19. The system of claim 18 wherein the highest priority one of the one or more local priority
2 values output from the priority storage array of the first CAM core constitutes the first
3 priority value, the highest priority one of the one or more local priority values output from
4 the priority storage array of the second CAM core constitutes the second priority value, and
5 the highest priority one of the one or more local priority values output from the priority

6 storage array of the third CAM core constitutes the third priority value.

1 20. The CAM device of claim 18 wherein each of the first, second and third CAM cores
2 comprises match lines coupled between the CAM array and the priority storage array, each
3 match line corresponding to a respective row of CAM cells within the CAM array; and
4 wherein each of the first, second and third CAM cores is further configured to generate
5 match signals on the match lines according to whether contents of the corresponding rows
6 of CAM cells match the comparand value, the match signals identifying the one or more
7 local priority values.

1 21. A content addressable memory (CAM) device comprising:
2 a CAM core to output a local priority number; and
3 a cascade logic circuit coupled to the CAM core to receive the local priority number and
4 having an input to receive at least one remote priority number from another CAM
5 device, the cascade logic circuit being configured to compare the local priority
6 number and the at least one remote priority number at one of a plurality of different
7 times according to a control value.

1 22. The CAM device of claim 21 further comprising a configuration circuit coupled to the
2 cascade logic to provide the control value thereto.

1 23. The CAM device of claim 22 wherein the configuration circuit comprises a programmable
2 non-volatile storage to store a configuration value, the configuration value including one or
3 more bits that correspond to the control value.

1 24. The CAM device of claim 22 wherein the configuration circuit is a one-time programmable

2 circuit.

1 25. The CAM device of claim 22 wherein the CAM core comprises an instruction decoder
2 being coupled to the configuration circuit and configured to store configuration information
3 within the configuration circuit in response to a configuration instruction from a host
4 device, the configuration information being value including one or more bits that
5 correspond to the control value.

1 26. The CAM device of claim 25 wherein the configuration instruction indicates includes
2 information that indicates a disposition of the CAM device within a hierarchy of
3 interconnected CAM devices.

1 27. The CAM device of claim 26 wherein the instruction decoder is configured to store, within
2 the configuration circuit, configuration information that indicates the one of the plurality of
3 different times in accordance with the disposition of the CAM device within the hierarchy
4 of interconnected CAM devices.

1 28. The CAM device of claim 21 further comprising an interface to receive the control value.

1 29. The CAM device of claim 28 wherein the interface comprises one or more integrated
2 circuit contacts.

1 30. A content addressable memory (CAM) device comprising:
2 a CAM core to generate a local priority value and corresponding match address; and
3 a cascade logic circuit coupled to receive the local priority value from the CAM core and
4 having an input to receive a first enable signal from a first other CAM device, the

5 cascade logic circuit being configured to compare the local priority value with a
6 remote priority value received from a second other CAM device and to output a
7 second enable signal to the second other CAM device if the remote priority value has
8 a higher priority than the local priority value, the cascade logic circuit being further
9 configured to enable the match address to be output from the CAM device if (1) the
10 local priority value has a higher priority than the remote priority value and (2) the
11 first enable signal is in a first state.

1 31. The CAM device of claim 30 further comprising a configuration circuit coupled to the
2 cascade logic circuit to provide a control value thereto, and wherein the cascade logic is
3 further configured to compare the local priority value with the remote priority value at a
4 time indicated by the control value.

1 32. The CAM device of claim 31 further comprising an instruction decoder coupled to the
2 configuration circuit and configured to store a configuration value therein in response to a
3 configuration instruction from a host device, the configuration value including one or more
4 bits that correspond to the control value.

1 33. The CAM device of claim 31 wherein the cascade logic circuit is further configured to
2 disable the match address from being output from the CAM device if remote priority value
3 has a higher priority than the local priority value or if the first enable signal is in a second
4 state.

1 34. The CAM device of claim 31 further comprising an output driver to output the match
2 address from the CAM device if a control signal generated by the cascade logic circuit is in

3 a drive-enable state, the cascade logic circuit being further configured to generate the
4 control signal in the drive-enable state if (1) the local priority value has a higher priority
5 than the remote priority value and (2) the first enable signal is in the first state.

1 35. A method of operation within a first content addressable memory (CAM) device, the
2 method comprising:
3 generating a local priority value and corresponding match address;
4 comparing the local priority value with a remote priority value received from a second
5 CAM device;
6 outputting an enable signal to the second CAM device if the remote priority value has a
7 higher priority than the local priority value; and
8 outputting the match address from the first CAM device if the local priority value has a
9 higher priority than the remote priority value and an enable signal is received from a
10 third CAM device.

1 36. The method of claim 35 wherein outputting the match address comprises outputting the
2 match address onto an output bus coupled to the first CAM device, second CAM device
3 and third CAM device.

1 37. The method of claim 35 wherein comparing the local priority value with the remote priority
2 value comprises comparing the local priority value with the remote priority value at one of
3 a plurality of different times indicated by a control value.

1 38. The method of claim 37 further comprising storing the control value in a configuration
2 circuit of the first CAM device.

1 39. The method of claim 38 wherein storing the control value in the configuration circuit
2 comprises storing the control value in the configuration circuit in response to a command
3 from a host device.

1 40. A method of operation within a content addressable memory (CAM) system, the method
2 comprising:
3 outputting a first priority value from a first CAM device;
4 comparing a second priority value with the first priority value within a second CAM device
5 and outputting a highest priority one of the first and second priority values; and
6 comparing a third priority value with the highest priority one of the first and second
7 priority values within a third CAM device and, if the highest priority one of the first
8 and second priority values has a higher priority than the third priority value,
9 outputting a first enable signal from the third CAM device to the second CAM
10 device.

1 41. The method of claim 40 further comprising outputting a second enable signal from the
2 second CAM device to the first CAM device if the first value has a higher priority than the
3 second value.

1 42. The method of claim 41 wherein outputting the second enable signal from the second CAM
2 device to the first CAM device comprises outputting the second enable signal from the
3 second CAM device to the first CAM device if (1) the first value has a higher priority than
4 the second value and (2) the first enable signal is output from the third CAM device to the
5 second CAM device.

1 43. The method of claim 41 further comprising:
2 generating a match address within the first CAM device, the match address corresponding
3 to the first priority value; and
4 outputting the match address onto a result bus coupled to the first, second and third CAM
5 devices if the second enable signal is output from the second CAM device to the first
6 CAM device.

1 44. The method of claim 41 wherein outputting the first enable signal from the third CAM
2 device to the second CAM device comprises outputting the first enable signal from the
3 third CAM device to the first and second CAM devices.

1 45. The method of claim 44 further comprising:
2 generating a match address within the first CAM device, the match address corresponding
3 to the first priority value; and
4 outputting the match address onto a result bus coupled to the first, second and third CAM
5 devices if (1) the second enable signal is output from the second CAM device to the
6 first CAM device and (2) the first enable signal is output from the third CAM device
7 to the first CAM device.

1 46. The method of claim 40 further comprising:
2 generating a match address within the second CAM device, the match address
3 corresponding to the second priority value; and
4 outputting the match address onto a result bus coupled to the first, second and third CAM
5 devices if (1) the first enable signal is output from the third CAM device to the

6 second CAM device and (2) the second priority value has a higher priority than the
7 first priority value.

1 47. The method of claim 40 further comprising:
2 generating a match address within the third CAM device, the match address corresponding
3 to the third priority value; and
4 outputting the match address onto a result bus coupled to the first, second and third CAM
5 devices if the third priority value has a higher priority than the highest priority one of
6 the first and second priority values.

1 48. The method of claim 40 wherein each of first, second and third priority values comprises a
2 respective N-bit value, N being an integer greater than one.

1 49. The method of claim 40 wherein outputting a highest priority one of the first and second
2 priority values comprises outputting a numerically lowest one of the first and second
3 priority values.

1 50. A content addressable memory (CAM) device comprising:
2 means for generating a local priority value and corresponding match address;
3 means for comparing the local priority value with a remote priority value received from a
4 first other CAM device;
5 means for outputting an enable signal to the first other CAM device if the remote priority
6 value has a higher priority than the local priority value; and
7 means for outputting the match address to an external signal path if the local priority value
8 has a higher priority than the remote priority value and an enable signal is received

9 from a second other CAM device.